Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit for executing a predetermined arithmetic operation with respect to the data read from memory;

a register for temporarily storing the data read from the memory; and

a combining circuit for ~~selecting one of~~ <u>receiving an output data from</u> the arithmetic logic unit and the register, and <u>outputting data which is provided by</u> replacing a part of the data read from the memory with <u>said received</u> output data ~~received from the selected one of the arithmetic logic unit and the register~~.

Claim 2 (Currently Amended): An arithmetic unit according to claim 1, wherein, when the part of the data read from the memory is replaced with an arithmetic result derived by the arithmetic logic unit, the combining circuit shifts [[the]] <u>a</u> position of data to be replaced by a predetermined number of bits every time an operation process is executed.

Claim 3 (Original): An arithmetic unit according to claim 1, wherein the memory

includes a plurality of memory blocks.

Claim 4 (Currently Amended): An arithmetic unit according to claim 1, wherein the

arithmetic logic unit ~~divide~~ divides a carry signal in response to a division signal

received thereto.

Claim 5 (Original): An arithmetic unit according to claim 1, further comprising a shifter

for shifting data received from the memory and outputting the shifted data to the

arithmetic logic unit.

Claim 6 (Original): An arithmetic unit according to claim 1, further comprising an

accumulator for temporary storing data output from the arithmetic logic unit.

Claim 7 (Currently Amended): An arithmetic unit comprising:

a memory for storing data;

an arithmetic logic unit capable of prohibiting ripple carry to an upper digit when

a carry signal instructs a carry at an arbitrary bit position;

a register capable of storing data to be used in the arithmetic logic unit before an

arithmetic operation is executed in the arithmetic logic unit; and

a combining circuit for ~~selecting one of~~ receiving an output data from the

arithmetic logic unit and the register, and <u>outputting data which is provided by</u> replacing

a part of the data read from memory with <u>said received</u> output data ~~received from the~~

~~selected one of the arithmetic logic unit and the register~~.

Claim 8 (Currently Amended): An arithmetic unit according to claim 7, wherein, when

the part of the data read from the memory is replaced with an arithmetic result derived

by the arithmetic logic unit, the combining circuit shifts [[the]] <u>a</u> position of data to be

replaced by a predetermined number of bits every time an operation process is

executed.

Claim 9 (Original): An arithmetic unit according to claim 7, wherein the memory

includes a plurality of memory blocks.

Claim 10 (Currently Amended): An arithmetic unit according to claim 7, wherein the

arithmetic logic unit ~~divide~~ <u>divides</u> a carry signal in response to a division signal

received thereto.

Claim 11 (Original): An arithmetic unit according to claim 7, further comprising a shifter

for shifting data received from the memory and outputting the shifted data to the

arithmetic logic unit.

Claim 12 (Original): An arithmetic unit according to claim 7, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.

Claim 13 (Currently Amended): An arithmetic unit comprising:

a memory for storing a plurality of data in a successive manner; and

a combining circuit for inserting unused data after data of a predetermined combination to makeup a bit shortage for subsequent data of a predetermined combination to start from a 0th or an 8th bit when data of the predetermined combination is narrower in width than 2^n-bit.

Claim 14 (Currently Amended): An arithmetic unit according to claim 13, further comprising an arithmetic logic unit for executing a predetermined arithmetic operation with respect to [[the]] data read from memory.

Claim 15 (Currently Amended): An arithmetic unit according to claim 13, further comprising a register for temporarily storing [[the]] data read from the memory.

Claim 16 (Currently Amended): An arithmetic unit according to claim 14, wherein, when [[the]] part of the data read from the memory is replaced with an arithmetic result derived by the arithmetic logic unit, the combining circuit shifts [[the]] a position of data to be replaced by a predetermined number of bits every time an operation process is

executed.

Claim 17 (Original): An arithmetic unit according to claim 13, wherein the memory includes a plurality of memory blocks.

Claim 18 (Currently Amended): An arithmetic unit according to claim 14, wherein the arithmetic logic unit ~~divide~~ <u>divides</u> a carry signal in response to a division signal received thereto.

Claim 19 (Original): An arithmetic unit according to claim 14, further comprising a shifter for shifting data received from the memory and outputting the shifted data to the arithmetic logic unit.

Claim 20 (Original): An arithmetic unit according to claim 14, further comprising an accumulator for temporary storing data output from the arithmetic logic unit.